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Group 2700

Sheet 1 of 2

37 CFR 1.501
INFORMATION DISCLOSURE STATEMENT
IN A PATENT
(use several sheets if necessary)

Docket No.	Serial No.
P99,0886	09/308,478
Applicants: Utz Wever, et al.	
Filing Date: May 17, 1999	Group Art Unit

U.S. PATENT DOCUMENTS

Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If appropriate
	AA						
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FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AL						X	
	AM							
	AN							
	AO							
	AP							
	AQ							
	AR							
	AS							

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AT	~~I. Hoefer, et al., *SPICE Analyseprogramm fur elektronische Schaltungen*, Springer, Berlin (1985), pp. 7-22~~
DWS	AU	U. Kleis, et al., *Domain Decomposition Methods for Circuit Simulation*, Proceedings of the 8th Workshop on Parallel and Distributed Simulation, PADS, Edinburgh, UK (July, 1994), pp. 183-86
DWS	AV	U. Wever, et al. *Parallel Transient Analysis for Circuit Simulation*, Proceedings of the 29th Annual Hawaii International Conference on System Sciences (1946), pp. 442-47
DWS	AW	B. Riess, et al., *Partitioning Very Large Circuits Using Analytical Placement Techniques*, Proceedings of the 31st ACM/IEEE Design Automation Conference (1994), pp. 646-51
DWS	AX	P. Johannes, *Partitioning of VLSI Circuits and Systems*, 33d Design and Automation Conference, Las Vegas (June 3-7, 1996), pp. 83-87

Examiner: Doug Sept | Date Considered: 4/30/01

***EXAMINER:** ~~Initial~~ if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

37 CFR 1.501
INFORMATION DISCLOSURE STATEMENT
IN A PATENT
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Docket No.	Serial No.
P99,0887	09/308,304
Applicants: Utz Wever, et al.	
Filing Date: May 17, 1999	Group Art Unit

U.S. PATENT DOCUMENTS

Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If appropriate
	BA						
	BB						
	BC						
	BD						
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	BF						
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	BH						
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FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	BL						X	
	BM							
	BN							
	BO							
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	BQ							
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DWS	BT	J. Cong, et al., *A Parallel Bottom-up Clustering Algorithm with Applications to Circuit Partitioning in VLSI Design*, In: 30th Design Automation Conference, June 14-18, 1993, pp. 755-760
DWS	BU	J. Li, et al., *New Spectral Linear Placement and Clustering Approach*, 33d Design Automation Conference, Las Vegas (June 3-7, 1996), pp. 88-93
DWS	BV	T. Kage, et al., *A Circuit Partitioning Approach for Parallel Circuit Simulation*, IEICE Trans Fundamentals, Vol. E77-A, No. 31 (1993), pp. 461-65
DWS	BW	G. Hung, et al., *Improving the Performance of Parallel Relaxation-Based Circuit Simulators*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, New York (November 12, 1993), No. 11, pp. 1762-74
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Examiner Doug Sery | Date Considered 4/30/01

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